

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

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APPLICANT(S): Sang-Hyun Lee and Deog-Kyoon Jeong
APPLICATION NO.: Not yet known
FILING DATE: Herewith
TITLE: DATA RECOVERY USING DATA EYE TRACKING
EXAMINER: Not yet known
GROUP ART UNIT: Not yet known
ATTY. DKT. NO.: 19570-05384

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner For Patents, Washington, D.C. 20231, on the date shown below:

Dated: Aug 29, 2001 By: Laura Majerus
Laura A. Majerus, Reg. No.: 33,417

COMMISSIONER FOR PATENTS
WASHINGTON, DC. 20231

INFORMATION DISCLOSURE STATEMENT
Under 37 CFR §§ 1.56 and 1.97-98

SIR:

Pursuant to the provisions of 37 CFR §§ 1.56 and 1.97-98, enclosed herewith is modified form PTO-1449 listing references for consideration by the Examiner. A copy is enclosed herewith of each listed reference, which may be material to the examination of this application, and with respect to which there may be a duty to disclose.

The filing of this Information Disclosure Statement shall not be construed as a representation regarding the completeness of the list of references, or that inclusion of a reference in this list is an admission that it is prior art or is pertinent to this application, or that a search has been made, or as an admission that the information listed is, or may be considered to be, material to patentability, or that no other material information exists, and shall not be construed as an admission against interest in any manner.

This application relies, under 35 U.S.C. § 120, on the earlier filing date of prior application Serial No. _____, filed on _____, and the

references cited therein are hereby referenced, but are not required to be provided in this application under 37 CFR § 1.98(d).

The Information Disclosure Statement submitted herewith is being filed:

- within three months of the filing date of the application, or date of entry into the national stage of an international application, or before the mailing date of a first official action on the merits, whichever event last occurred;
OR
- before the mailing of a first official action after the filing of a request for continued examination (RCE) under 37 CFR § 1.114;
- after three months of the filing date of this national application or the date of entry of the national stage in an international application, or after the mailing date of the first official action on the merits, whichever event last occurred, but before the mailing date of the first to occur of either:
 - (1) a final action under 37 CFR § 1.113; OR
 - (2) a notice of allowance under 37 CFR § 1.311; AND
 - attached hereto is the fee of \$180, as set forth under 37 CFR § 1.17(p), for submission of this Information Disclosure Statement under 37 CFR § 1.97(c); OR
 - Applicant certifies pursuant to 37 CFR § 1.97(e) that:
 - each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Statement;
OR
 - no item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the person signing this certification after making reasonable inquiry, was known to any individual designated under 37 CFR § 1.56(c) more than three months prior to the filing of this Statement.

OR

- before the payment of the issue fee but after the mailing date of the first to occur of either:
 - [1] a final action under 37 CFR § 1.113; OR

[2] a notice of allowance under 37 CFR § 1.311; AND
in accordance with the requirements of 37 CFR § 1.97(d):

Applicant certifies pursuant to 37 CFR. § 1.97(e) that:

each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Statement;
OR

no item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the person signing this certification after making reasonable inquiry, was known to any individual designated under 37 CFR § 1.56(c) more than three months prior to the filing of this Statement; AND

Applicant hereby respectfully petitions for the consideration of the accompanying Information Disclosure Statement under 37 CFR § 1.97(d)(2); AND

Applicant submits the petition fee of \$180 as set forth in 37 CFR § 1.17(p).

Applicant submits that no fee is required for the consideration of the accompanying Information Disclosure Statement.

Consideration of the listed references and favorable action are solicited.

Respectfully submitted,
SANG-HYUN LEE AND DEOG-KYON JEONG

Dated: Aug 29, 2001

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FORM PTO-1449 (REV. 6-89)		U.S. DEPARTMENT OF COMMERCE Patent and Trademark Office		Attorney's Docket No. 19570-05384	Serial No. To Be Assigned
INFORMATION DISCLOSURE CITATION				Applicant Sang-Hyun Lee and Deog-Kyoon Jeong	
(Use several sheets if necessary)				Filing Date Herewith	Group Art Unit To Be Assigned



U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	A	4,218,771	8/19/80	Hogge, Jr.	375	120	12/4/78
	B	4,584,695	4/22/86	Wong et al.	375	81	11/9/83
	C	4,821,297	4/11/89	Bergmann et al.	375	120	11/19/87
	D	5,432,480	7/11/95	Popescu	331	11	4/8/93
	E	5,481,563	1/2/96	Hamre	375	226	3/14/94
	F	5,554,945	9/10/96	Lee et al.	327	105	2/15/94
	G	5,870,445	2/9/99	Farwell	375	371	12/27/95

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

H	Maneatis, John G., "Low-Jitter Process Independent DLL and PLL Based on Self-Biased Techniques," IEEE Journal of Solid-State Circuits, pp.1723-1732, No.11, November 1996
I	Rau, M. et al., "Clock/Data Recovery PLL Using Half-Frequency Clock," IEEE Journal of Solid-State Circuit, pp.1156-1160, No. 7, July 1997
J	Poulton, John et al., "A Tracking Clock Recovery Receiver for 4GBPS Signaling," IEEE Micro, pp.25-26, Jan-Feb 1998

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if references considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered.
Include copy of this form with next communication to applicant.